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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,465	07/23/2004	Androula G. Nassiopoulou	30848/40323	3973

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EXAMINER	
ROSENBERGER, FREDERICK F	
ART UNIT	**PAPER NUMBER**
2884	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/502,465	NASSIOPOULOU ET AL.	
	Examiner	Art Unit	
	Frederick F. Rosenberger	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39 and 40* is/are allowed.

6)☒ Claim(s) *31* is/are rejected.

7)☒ Claim(s) *32-38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's reply, filed 9 August 2006, has been received and entered. Accordingly, changes have been made to the specification. Claims 1-30 have been cancelled. Claims 31-40 have been added. Thus, claims 31-40 are currently pending in this application.

Claim Objections

2. Claims 38 and 40 are objected to because of the following informalities:

In claim 38, the first line of subheading (f)(i), "a polysilicon layer" probably should be --a first polysilicon layer-- to establish proper antecedent basis for the rest of the claim.

In claim 38, the second line of subheading (h), "the microfluidic channel" lacks proper antecedent basis.

In claim 38, lines 2-3 of subheading (i), "the microfluidic channel" lacks proper antecedent basis.

In claim 40, line 3 of subheading (g), "or" should probably be --and-- to indicate that the group consists of the elements specified inclusive.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tjerkstra et al. (Journal paper entitled "Multi-Walled Microchannels: Free-Standing Porous Silicon Membranes for Use in μTAS") in view of Nassiopoulos (Section from Properties of Porous Silicon entitled "Local Formation and Patterning of Porous Silicon").

With regards to claim 31, Tjerkstra et al. teach a silicon processing method comprising the steps of:

(a) providing a silicon substrate comprising a top side, a bottom side, and a bulk region (Figure 4; page 495, section II, paragraph 3);

(b) forming an ohmic contact anode on the bottom side of the silicon substrate, in the form of a 750-nm layer of aluminum (page 496, section III(A), paragraph 1);

(c) forming a masking layer of silicon nitride on the top side of the silicon substrate and then patterning the layer to expose a portion of the substrate (page 496, section III(A), paragraph 1);

(d) forming a sealed microchannel by performing an electrochemical process comprising:

(i) anodizing with a first current density below the critical value for electropolishing, thereby forming a porous silicon capping layer in the exposed portion of the top side of the silicon substrate (Figures 3 and 4; page 495, section II, paragraphs 2 and 3);

(ii) anodizing with a second current density above the critical value for electropolishing, thereby dissolving a portion of the silicon substrate and forming a microchannel below the porous silicon capping layer (Figures 3 and 4; page 496, section III(A), paragraph 4).

Although Tjerkstra discloses substantially similar process steps as the presently claimed invention, Tjerkstra is silent with regards to the masking layer comprising a bilayer of silicon dioxide and polycrystalline silicon (also commonly referred to as polysilicon). Instead, Tjerkstra discloses a silicon nitride masking layer.

However, it is well known that the double layer of silicon dioxide and polysilicon can be used as a masking layer for porous silicon formation. For example, Nassiopoulos teaches that photoresists, silicon dioxide, silicon nitride, silicon carbide,

and metals can be used as masks for local anodization in the formation of porous silicon (section B, page 77). Nassiopoulos further discloses that a polysilicon layer combined on top of a silicon dioxide layer (SiO_2) shows the best masking characteristics (last line of section B). In the table on page 78, Nassiopoulos further illustrates that a bilayer of polysilicon and silicon dioxide has the further advantage over other masking materials of having an infinite maximum anodization time. Thus, it would have been obvious for a person having ordinary skill in the art at the time the invention was made to use a bilayer of polysilicon and silicon dioxide for the masking material instead of silicon nitride since the bilayer of polysilicon and silicon dioxide shows the best masking characteristics and the greatest maximum anodization time of known masking materials, as taught by Nassiopoulos.

It is noted that the process employed by Tjerkstra generates a sealed microchannel by virtue of the porous layer being held at the borders of the porous layer region, thereby allowing a sealed region to exist below the porous silicon layer, as illustrated in Figures 1-4.

6. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lammel et al. (Journal paper entitled "Free-standing, mobile 3D porous silicon microstructures") in view of Halimaoui (Section from Properties of Porous Silicon entitled "Porous Silicon Formation by Anodisation") and Nassiopoulos (Section from Properties of Porous Silicon entitled "Local Formation and Patterning of Porous Silicon").

With regards to claim 31, Lammel et al. teach a silicon processing method comprising the steps of:

(a) providing a silicon substrate comprising a top side, a bottom side, and a bulk region (Figures 1 and 3);

(b) forming an ohmic contact using platinum electrodes immersed in HF/ethanol solution (Figure 1);

(c) forming a masking layer of metal and then patterning the masking layer, exposing a portion of the top side of the silicon substrate (section 2.2; Figure 3);

(d) forming a sealed microchannel by performing an electrochemical process comprising:

(i) anodizing with a first current density below the critical value for electropolishing to form a porous silicon capping layer in the exposed portion of the top side of the silicon substrate (section 2.3; Figures 2 and 3);

(ii) anodizing with a second current density above the critical value for electropolishing, thereby dissolving a portion of the silicon and forming a microchannel region below the porous silicon layer (section 2.4; Figure 4).

Although Lammel discloses substantially similar process steps as the presently claimed invention, Lammel is silent with regards to two aspects: the masking layer comprising a bilayer of silicon dioxide and polycrystalline silicon (also commonly referred to as polysilicon) and the ohmic contact anode formed on the bottom side of the substrate. Instead, Lammel disclose a metallic masking layer and anode separate from the silicon substrate, respectively.

With regards to the contact anode, it is a well-known variation for the formation of porous silicon to use the silicon wafer as the anode, wherein the backside of the silicon wafer has been metallized to provide electrical contact thereto. Halimaoui teaches such a configuration. On page 12, Halimaoui teaches that the configuration with the silicon wafer as the anode (Figure 1) has the advantage of simplicity and the ability to anodize different silicon structures. On page 13, Halimaoui discusses the double tank cell configuration (Figure 3) employed by Lammel et al. Specifically, the double tank cell configuration allows for the backside of the silicon wafer to be non-metallized, but requires high-dose implantation. Thus, it would have been obvious for a person having ordinary skill in the art at the time the invention was made to form an ohmic contact anode on the bottom of the silicon substrate instead of using a separate anode in the double tank cell anodization of Lammel et al., since such a configuration is well known in the art and provides a simpler structure compared to the double tank configuration, as taught by Halimaoui.

With regards to the masking layer, it is further well known that the double layer of silicon dioxide and polysilicon can be used as a masking layer for porous silicon formation. For example, Nassiopoulos teaches that photoresists, silicon dioxide, silicon nitride, silicon carbide, and metals can be used as masks for local anodization in the formation of porous silicon (section B, page 77). Nassiopoulos further discloses that a polysilicon layer combined on top of a silicon dioxide layer (SiO_2) shows the best masking characteristics (last line of section B). In the table on page 78, Nassiopoulos further illustrates that a bilayer of polysilicon and silicon dioxide has the further

advantage over other masking materials of having an infinite maximum anodization time. Thus, it would have been obvious for a person having ordinary skill in the art at the time the invention was made to use a bilayer of polysilicon and silicon dioxide for the masking material instead of metal since the bilayer of polysilicon and silicon dioxide shows the best masking characteristics and the greatest maximum anodization time of known masking materials, as taught by Nassiopoulos.

It is noted that the process employed by Lammel generates a sealed microchannel by virtue of the porous layer being held at the borders of the porous layer region, thereby allowing a sealed region to exist below the porous silicon layer.

Response to Arguments

7. Applicant's arguments with respect to claim 31 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

8. Claims 39 and 40 are allowed.

9. Claims 32-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

With regards to claims 32, 35, and 38, the obviousness combination of Kaltsas and Lammel cited in the previous action would constitute the closest prior art for the claimed silicon processing method. Based on the arguments provided by applicant (see the response filed 9 August 2006, page 11 – top of page 12), the examiner agrees that the combination of said references to achieve the claimed invention would not have been obvious. Kaltsas does not teach the formation of a microchannel below the porous silicon capping layer, while both Lammel and Tjerkstra fail to teach any processing steps leading to the formation of a heater, thermocouples, or resistors on the porous silicon layer. Claims 33, 34, 36, and 37 would be allowable by virtue of their dependency on claims 32 and 35.

With regards to claim 39, the prior art of record fails to teach or reasonably suggest a porous silicon capping layer locally formed above a microchannel with the claimed layout of the sensor elements in combination with the other claimed elements of the thermal flow sensor. The closest prior art, Kaltsas, fails to teach a microchannel formed below the porous silicon layer.

With regards to claim 40, the prior art of record fails to teach or reasonably suggest a porous silicon capping layer locally formed above a microchannel with the claimed layout of microfluidic sensor. The closest prior art, Kaltsas, fails to teach a microchannel formed below the porous silicon layer.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Artmann et al. (US Patent # 6,759,265) teach a method for producing a porous silicon diaphragm for a thermocouple-based sensor, but fail to disclose the specifics of the claimed silicon processing method, the thermal flow sensor, or the thermal microfluidic sensor.

Benzel et al. (US Patent # 6,832,523) teach a device with a sealed cavity and a porous silicon membrane with thermocouple-based sensors, but fail to disclose the specifics of the claimed silicon processing method, the thermal flow sensor, or the thermal microfluidic sensor.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frederick F. Rosenberger whose telephone number is 571-272-6107. The examiner can normally be reached on Monday-Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on 571-272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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